CLAIMS

What is claimed is:

1. A system, comprising:

a first application specific integrated circuit;

a first random access memory coupled with the first application specific integrated circuit;

a first memory testing engine to execute test operations on the first random access memory;

a first bus slave controller coupled with the first memory testing engine to provide access to the first random access memory;

a processor to control the first bus slave controller; and

a bus to connect the processor to the first bus slave controller.

2. The system of claim 1, further comprising:

a second application specific integrated circuit;

a second random access memory coupled with the second application specific integrated circuit;

a second memory testing engine to execute test operations on the second random access memory, the second memory testing engine controlled by the processor via the bus; and

a second bus slave controller coupled with the second memory testing engine to provide access to the second random access memory.

3. The system of claim 2, wherein the first and second memory testing engine perform testing operations concurrently.

4. The system of claim 1, wherein the memory test engine is integrated with the slave bus controller.

5. The system of claim 1, wherein the memory test engine generates test data and expected responses.

6. The system of claim 5, wherein the memory test engine captures and compares an actual random access memory response to the test data.

7. The system of claim 1, wherein the memory test engine is responsible for programmable address ranges and data widths.

8. The system of claim 1, wherein the memory test engine tests memory in an incrementing memory address order.

9. The system of claim 1, wherein the memory test engine tests memory in a decrementing memory address order.

10. The system of claim 1, wherein the memory test engine tests memory in single address mode.

11. The system of claim 1, wherein the memory test engine tests memory in burst/block mode.

12. The system of claim 1, wherein the memory test engine saves a failing address for the processor.

13. The system of claim 1, wherein the memory test engine saves a failing data value for the processor.

14. The system of claim 1, wherein the memory test engine discontinues an active test until the processor reads a failing address and a memory address location.

15. The system of claim 1, wherein the memory test engine reports an asynchronous interrupt to the processor.

16. A method, comprising:

transmitting an initiation signal from a processor via a bus to a first memory testing engine coupled with a first application specific integrate circuit via a first bus slave controller; and

testing a first random access memory associated with the first integrated circuit using the first memory testing engine.

17. The method of claim 16, further comprising:

transmitting an initiation signal from the processor via the bus to a plurality of memory testing engines, each coupled with an application specific integrate circuit via a bus slave controller; and

testing a random access memories associated with the integrated circuit using the memory testing engine.

18. The method of claim 17, wherein testing by the plurality of memory testing engines is concurrent.

19. The method of claim 16, further comprising generating test data and expected responses.

20. The method of claim 19, further comprising capturing and comparing an actual random access memory response to the test data.

21. The method of claim 16, wherein testing comprises writing multiple data patterns per a memory location within the first random access memory and comparing a reading of the location with an expected response.

22. The method of claim 16, further comprising testing memory in an incrementing memory address order.

23. The method of claim 16, further comprising testing memory in a decrementing memory address order.

24. The method of claim 16, further comprising testing memory in single address mode.

25. The method of claim 16, further comprising testing memory in burst/block mode.

26. The method of claim 16, further comprising saving a failing address for the processor.

27. The method of claim 16, further comprising saving a failing data value for the processor.

28. The method of claim 16, further comprising discontinuing an active test until the processor reads a failing address and a memory address location.

29. The method of claim 16, further comprising reporting an asynchronous interrupt to the processor.

30. A machine-readable storage medium tangibly embodying a sequence of instructions executable by the machine to perform a method comprising:

transmitting an initiation signal from a processor via a bus to a first memory testing engine coupled with a first application specific integrate circuit via a first bus slave controller; and

testing a first random access memory associated with the first integrated circuit using the first memory testing engine.

31. The machine-readable storage medium of claim 30, further comprising:

transmitting an initiation signal from the processor via the bus to a plurality of memory testing engines, each coupled with a application specific integrate circuit via a bus slave controller; and

testing a random access memory associated with the integrated circuit using the memory testing engine.

32. The machine-readable storage medium of claim 31, wherein testing by the plurality of memory testing engines is concurrent.

33. The machine-readable storage medium of claim 30, further comprising generating test data and expected responses.

34. The machine-readable storage medium of claim 33, further comprising capturing and comparing an actual random access memory response to the test data.

35. The machine-readable storage medium of claim 30, wherein testing comprises writing multiple data patterns per a memory location within the first random access memory and comparing a reading of the location with an expected response.

36. The machine-readable storage medium of claim 30, further comprising testing memory in an incrementing memory address order.

37. The machine-readable storage medium of claim 30, further comprising testing memory in a decrementing memory address order.

38. The machine-readable storage medium of claim 30, further comprising testing memory in single address mode.

39. The machine-readable storage medium of claim 30, further comprising testing memory in burst/block mode.

40. The machine-readable storage medium of claim 30, further comprising saving a failing address for the processor.

41. The machine-readable storage medium of claim 30, further comprising saving a failing data value for the processor.

42. The machine-readable storage medium of claim 30, further comprising discontinuing an active test until the processor reads a failing address and a memory address location.

43. The machine-readable storage medium of claim 30, further comprising reporting an asynchronous interrupt to the processor.

44. An apparatus comprising:

a means for transmitting an initiation signal from a processor via a bus to a first memory testing engine coupled with a first application specific integrate circuit via a first bus slave controller; and

a means for testing a first random access memory associated with the first integrated circuit using the first memory testing engine.

45. The apparatus of claim 44, further comprising:

a means for transmitting an initiation signal from the processor via the bus to a second memory testing engine coupled with a second application specific integrate circuit via a second bus slave controller; and

a means for testing a second random access memory associated with the second integrated circuit using the second memory testing engine.

46. The apparatus of claim 45, wherein testing by the first and second memory testing engine is concurrent.

47. The apparatus of claim 44, further comprising a means for generating test data and expected responses.

48. The apparatus of claim 47, further comprising a means for capturing and comparing an actual random access memory response to the test data.

49. The apparatus of claim 44, wherein testing comprises writing multiple data patterns per a memory location within the first random access memory and comparing a reading of the location with an expected response.

50. The apparatus of claim 44, further comprising a means for testing memory in an incrementing memory address order.

51. The apparatus of claim 44, further comprising a means for testing memory in a decrementing memory address order.

52. The apparatus of claim 44, further comprising a means for testing memory in single address mode.

53. The apparatus of claim 44, further comprising a means for testing memory in burst/block mode.

54. The apparatus of claim 44, further comprising a means for saving a failing address for the processor.

55. The apparatus of claim 44, further comprising a means for saving a failing data value for the processor.

56. The apparatus of claim 44, further comprising a means for discontinuing an active test until the processor reads a failing address and a memory address location.

57. The apparatus of claim 44, further comprising a means for reporting an asynchronous interrupt to the processor.